XVIII Polish Workshop on Relativistic Heavy-Ion Collisions
Strange and Heavy Flavour Physics

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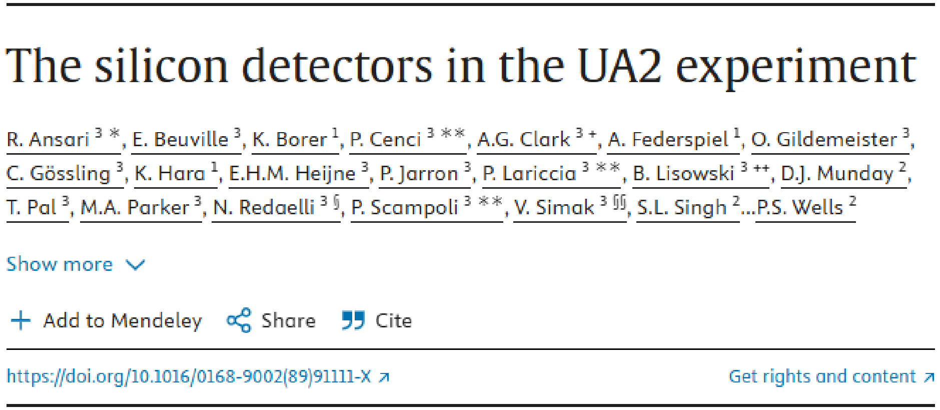
13-14 Dec 2025
Jagiellonian University

Some thoughts on Silicon Pixel Detectors, disorganized, still hopefully interesting, reflecting the very own point of view of the speaker

P. Martinengo
CERN

Pixel detectors are widely use in HEP since more than 25 years
I won’t try to convince you that 2-D is better than 1-D and why

In 1988 UA2 operated
for the first time a Si Detector, pitch 17.3 mm x 33.5 mm,
perhaps the first modern (pixel ?) 2-D Vertex Detector



The silicon detectors in the UA2 experiment

R. Ansari[3 *], E. Beuville[3], K. Borer[1], P. Cenci[3 **], A.G. Clark[3 +], A. Federspiel[1], O. Gildemeister[3], C. Gössling[3], K. Hara[1], E.H.M. Heijne[3], P. Jarron[3], P. Lariccia[3 **], B. Lisowski[3 ++], D.J. Munday[2], T. Pal[3], M.A. Parker[3], N. Redaelli[3 §], P. Scampoli[3 **], V. Simak[3 §§], S.L. Singh[2]...P.S. Wells[2]

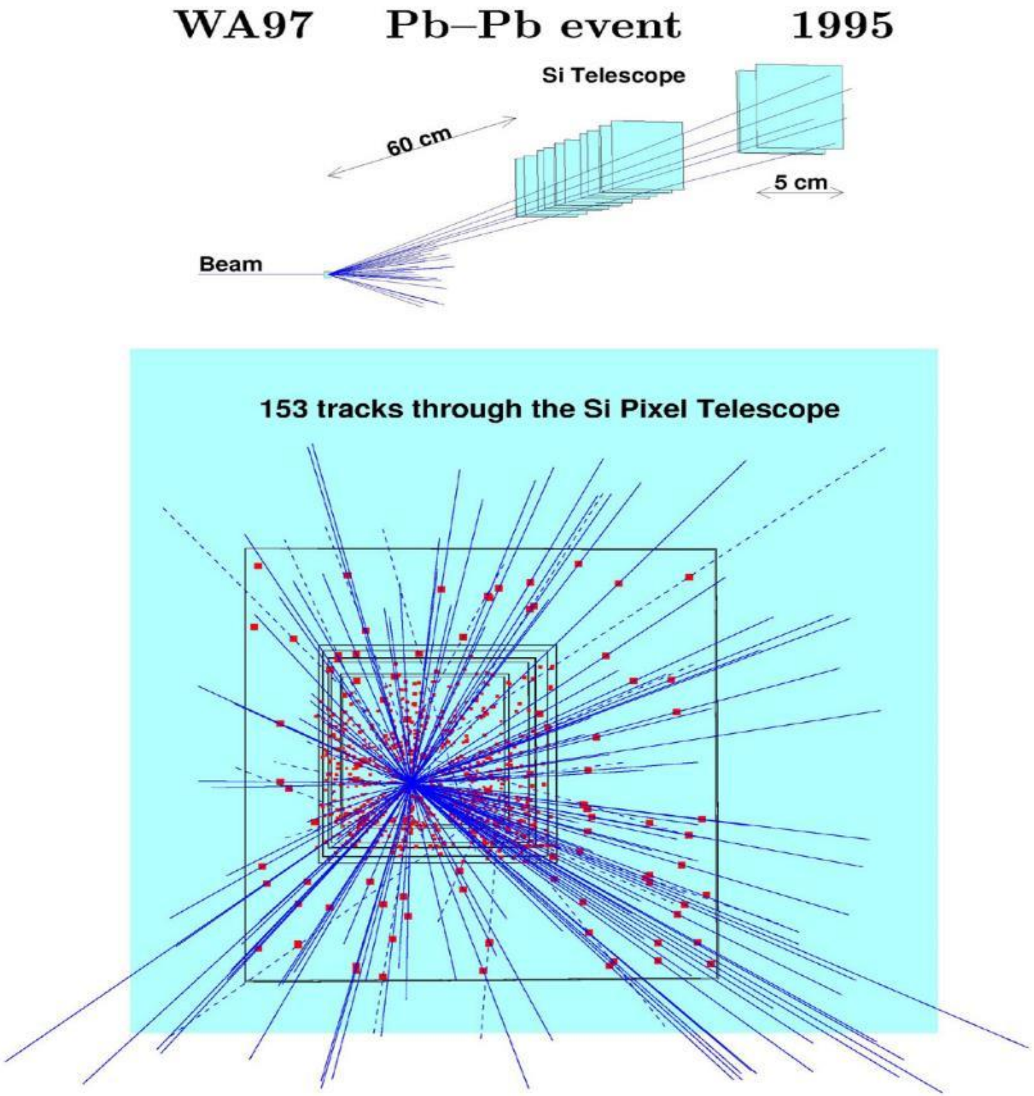
https://doi.org/10.1016/0168-9002(89)91111-X

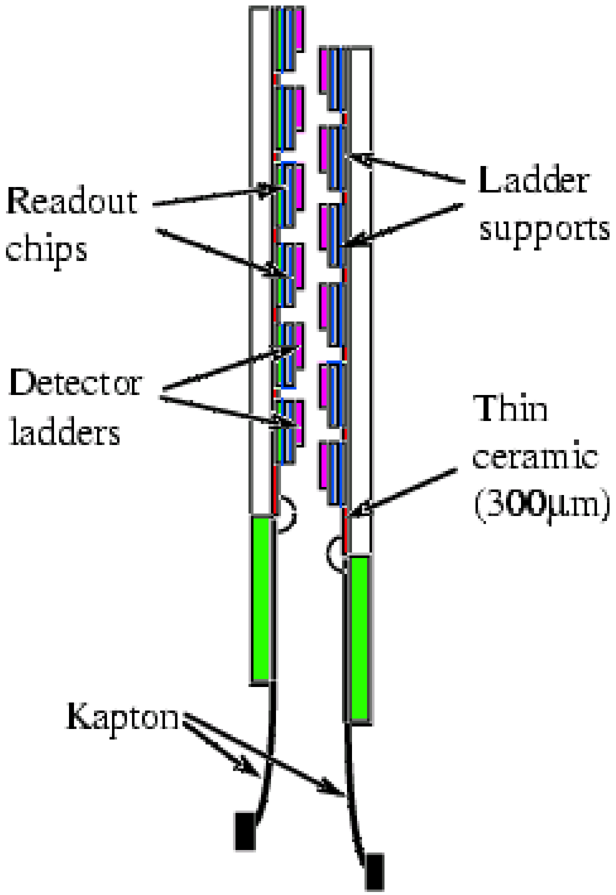
I will try to outline some aspects of Silicon Pixel Detectors that are, IMO, interesting more than, explaining how wonderful SPDs are

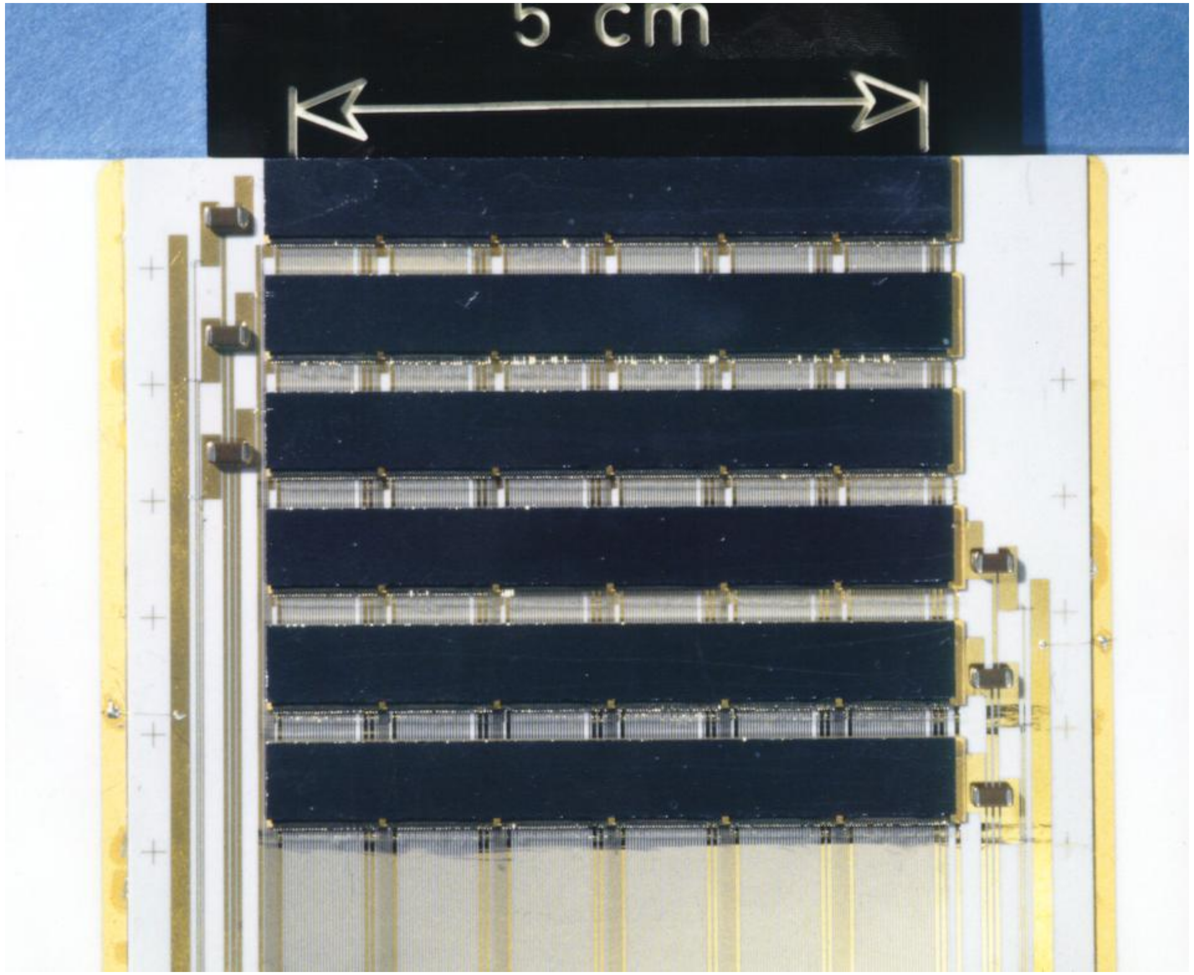
I will take ALPIDE (ALice PIxel DEtector) as reference/example
because I know a bit of it, it is used in ALICE but also in NA61
(and in the sPHENIX MVTX)
I hope my presentation will be more general

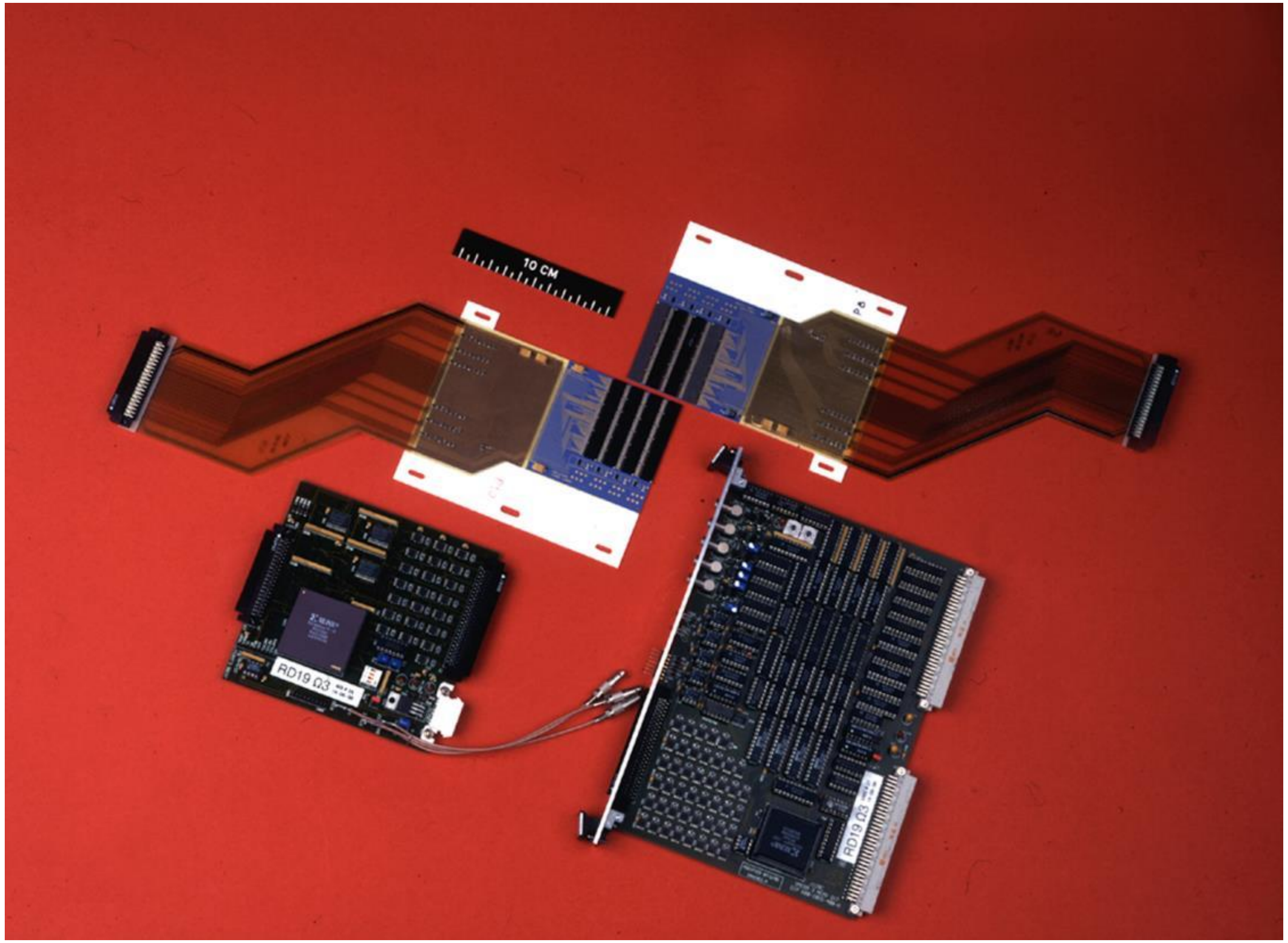
In the slides you will find links to presentations by true experts
Likely they are the most useful & interesting part of this talk

In 1995 the WA97 experiment operated the first pixel telescope in Pb-Pb collisions (fixed target mode)




Readout chips
Detector ladders
Kapton
Ladder supports
Thin ceramic (300µm)


5 cm



The WA97 telescope consisted of 7 planes, 50 mm x 50 mm active area

0.5 x 10^6 pixels in total

Omega2/3

50 um x 500 um (0.5 x 10^6 in total)

25 years

ALPIDE (ALICE ITS2 & NA61)

25 um x 25 um (12 x 10^9 in total)

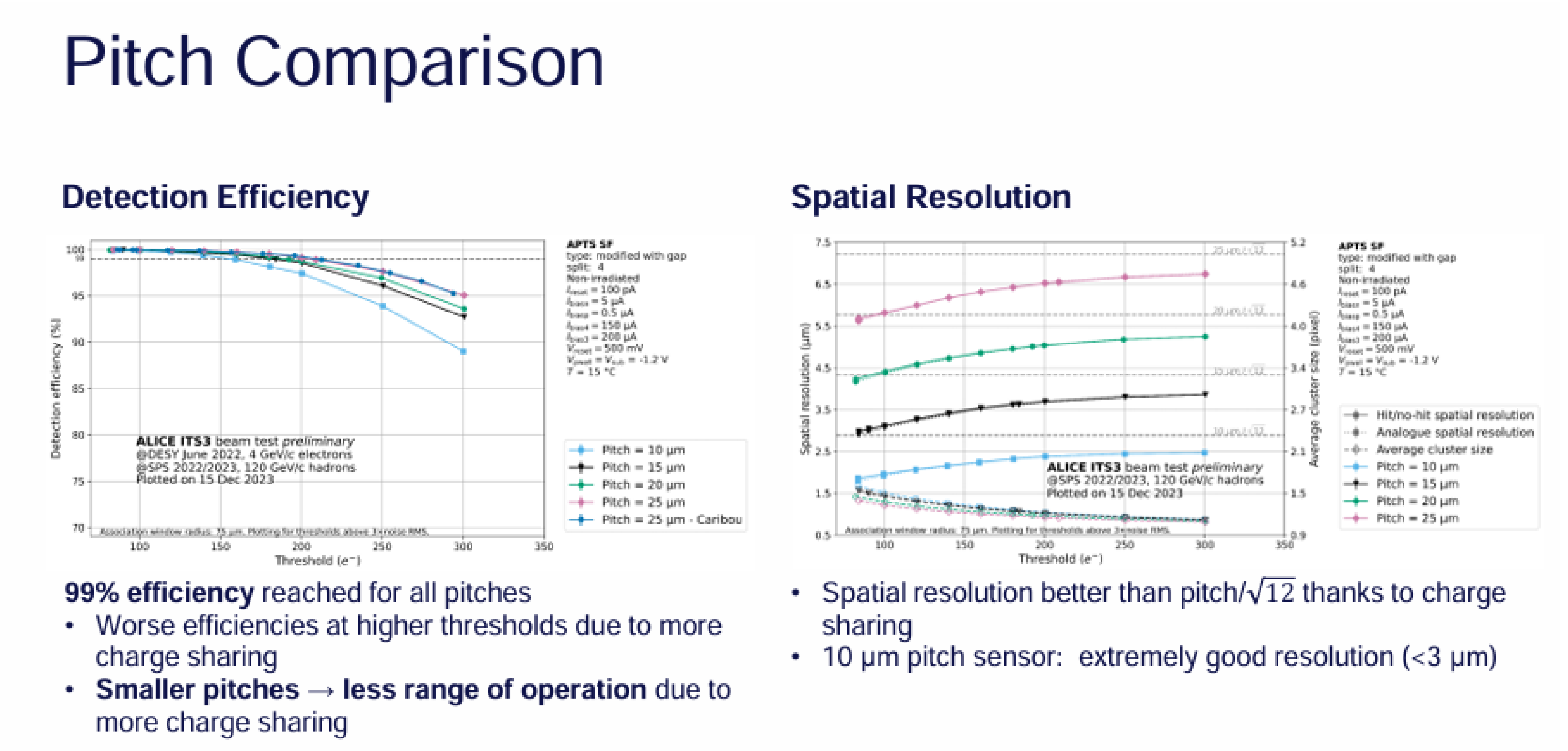
(1 pixel in Omega = 40 pixels in ALPIDE)

WHAT NEXT ?

Well, smaller and smaller, of course

[Characterisation of analogue Monolithic Active Pixel Sensor test structures implemented in a 65 nm CMOS imaging process](https://cds.cern.ch/record/2893905/files/2403.08952.pdf)

https://cds.cern.ch/record/2893905/files/2403.08952.pdf



Pitch Comparison

Detection Efficiency

99% efficiency reached for all pitches

- Worse efficiencies at higher thresholds due to more charge sharing
- **Smaller pitches → less range of operation** due to more charge sharing

Spatial Resolution

- Spatial resolution better than pitch/$\sqrt{12}$ thanks to charge sharing
- 10 μm pitch sensor: extremely good resolution (<3 μm)

Not a claim this is the only or best development !

Is the pixel pitch the limiting factor ?

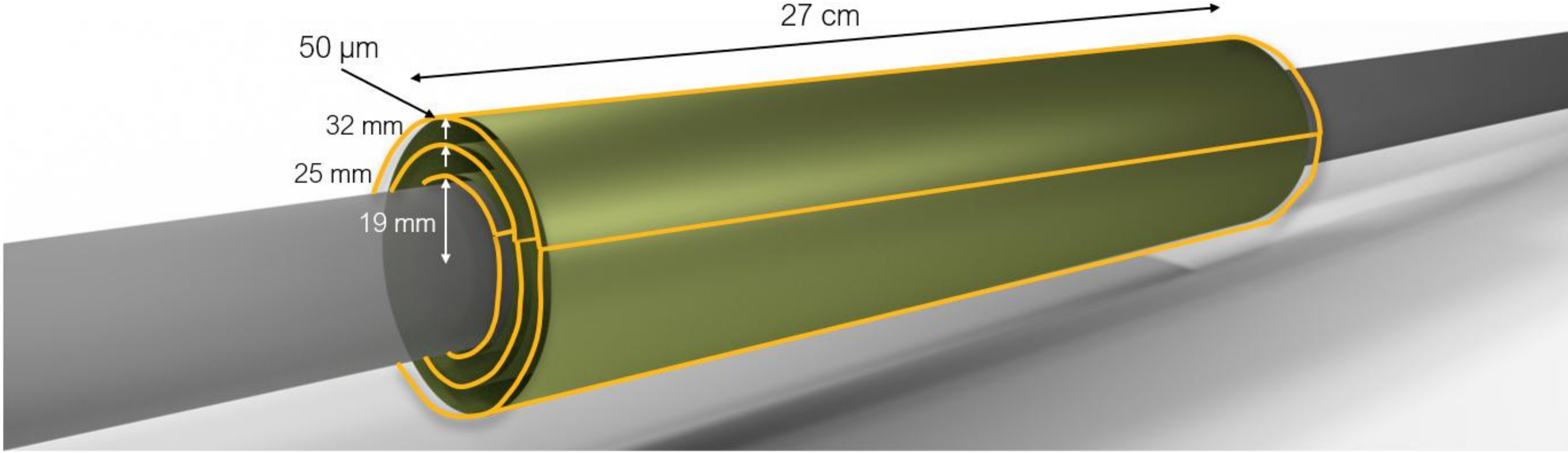
Not sure

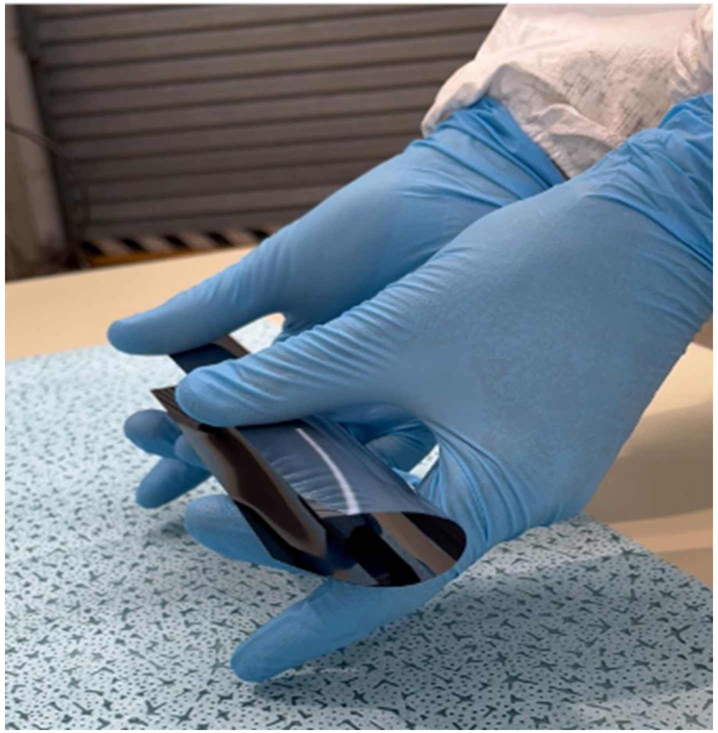
ALICE ITS3 concept

A. Kluge, ALICE ITS3 - A bent wafer-scale monolithic pixel detector (11 April 2025) · Indico

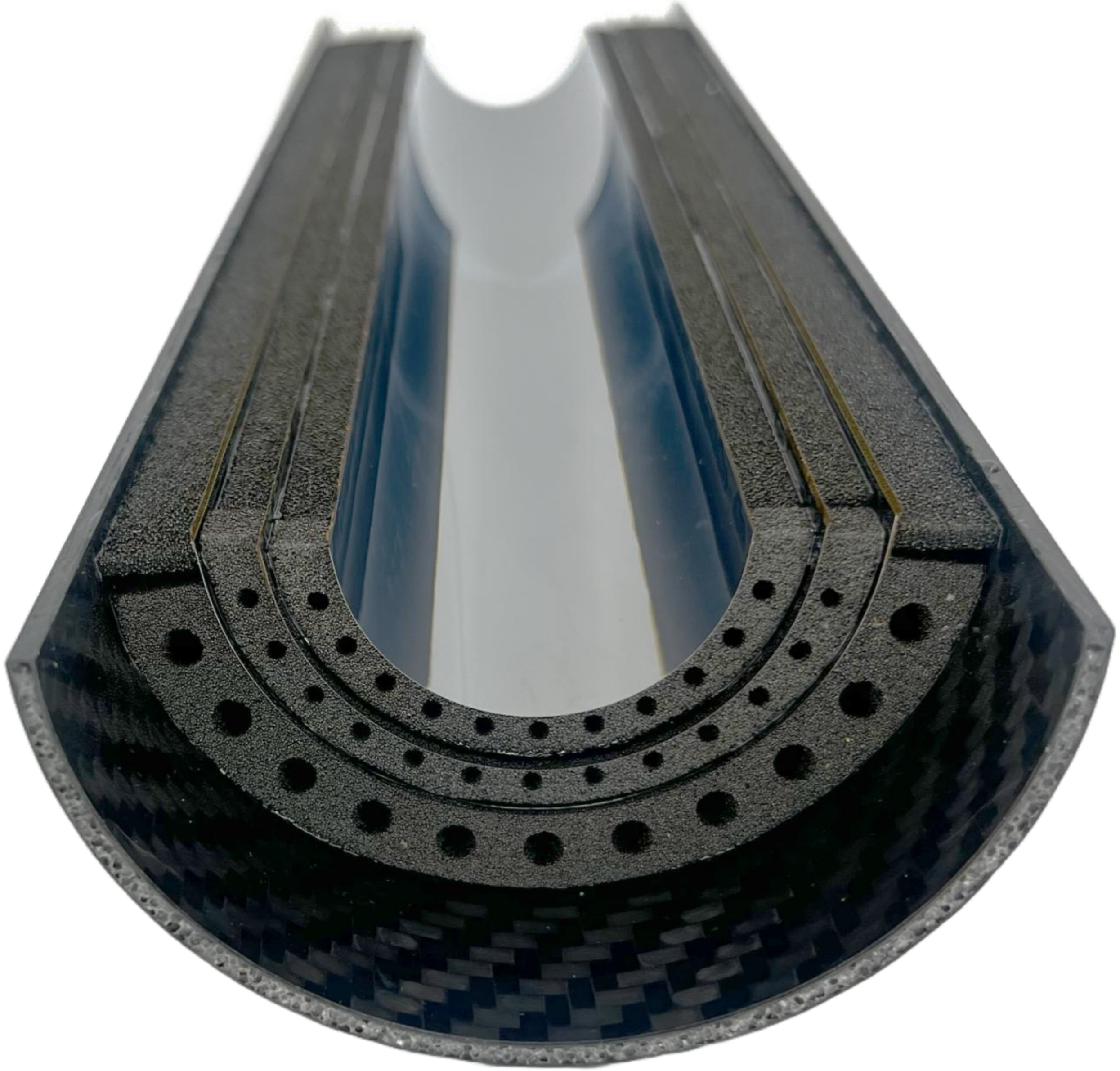
3 half barrels 1st layer 24 mm → 19 mm
6 x 27 cm long sensors – bent around beam pipe
Pixel pitch 22.8 um x 20.8 um

No rigid support structure: Carbon fiber foam spacers
Air cooled
No flexible printed circuit over sensor for signal and power

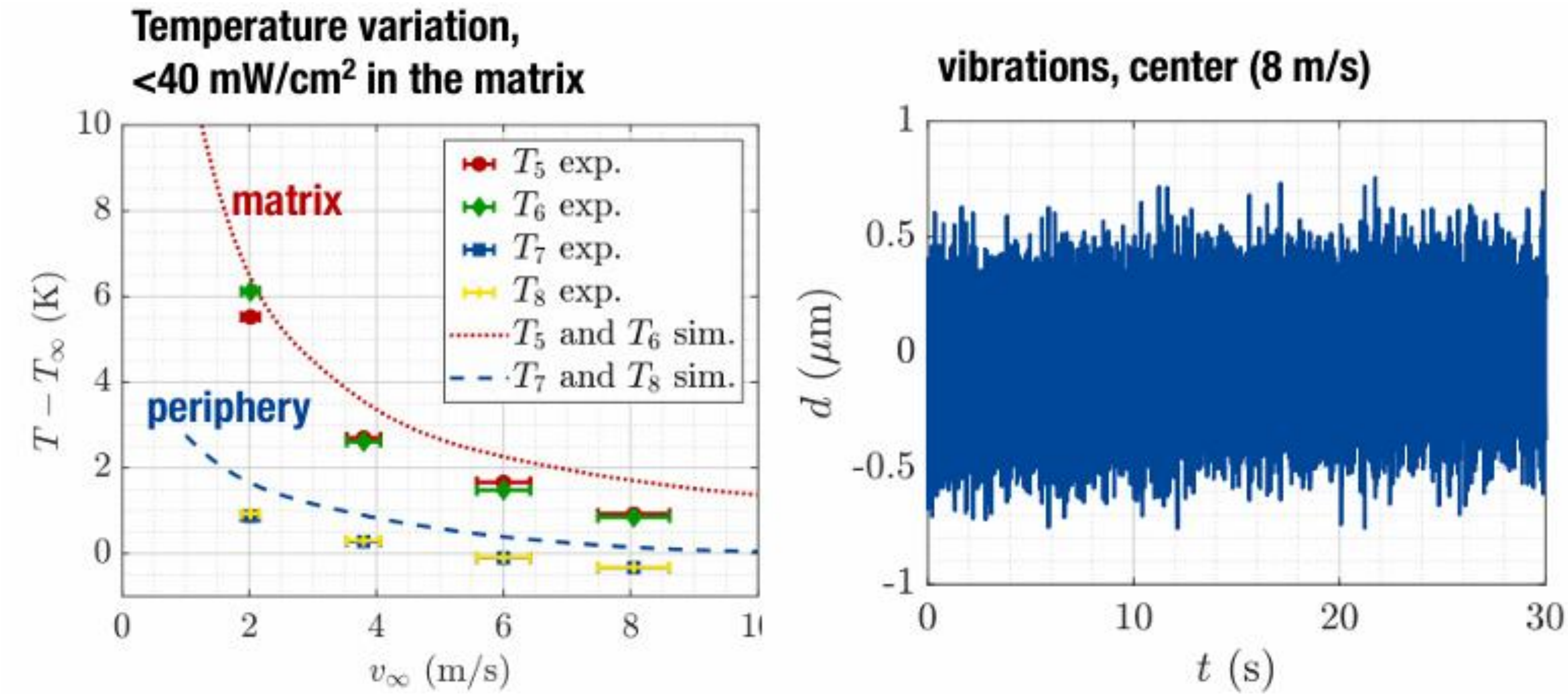




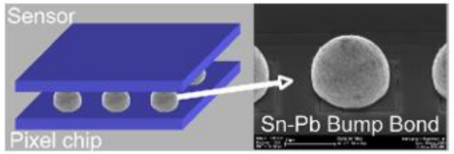
ITS3 TDR, CERN-LHCC-2024-003, https://cds.cern.ch/record/2890181



Vibration induced by air cooling (ALICE ITS3 development)

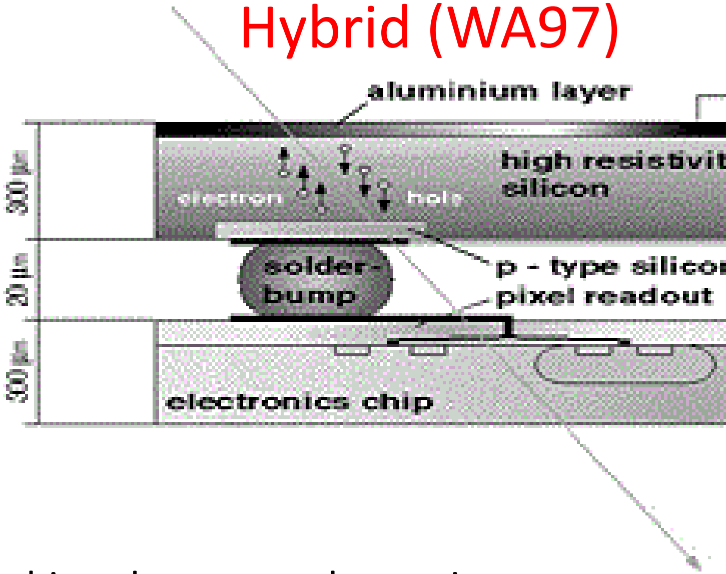


Alignment, mechanical/termal stability etc. may eventually be the limiting factor



Hybrid vs. Monolithic

Hybrid (WA97)



Two different chips, detector + electronics:

+ flexible (detector material can be different from Si), higher resistivity (SiC, GaAS, CdTe) and thickness can be tuned

- extra production step, yield

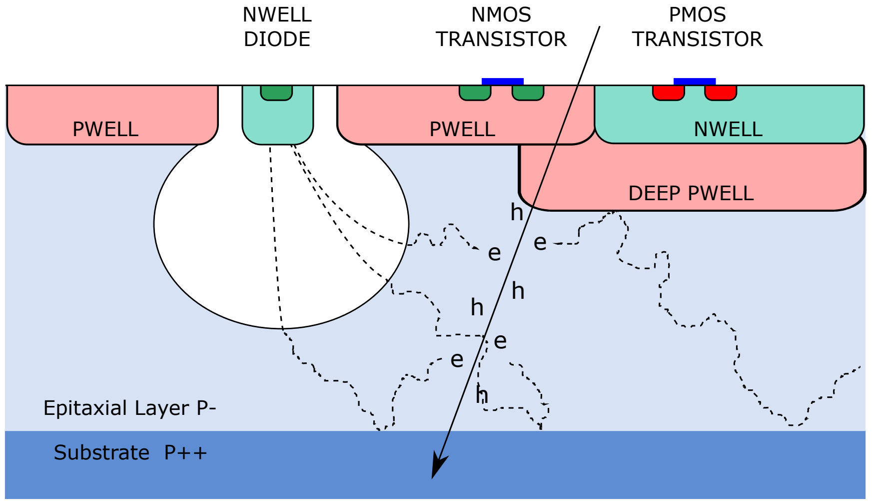
- thicker, more material

+ no constraints on electronics design (but bump), 100% fill factor

+ no issue with back bias, full depletion possible (more robust w.r.t. radiation damage)

+ Mature technology, present in all LHC experiment

Monolithic (ALPIDE)



One chip, detector + electronics on the same substrate:

+ thinner, less material (down to 50 μm)

+ one production step

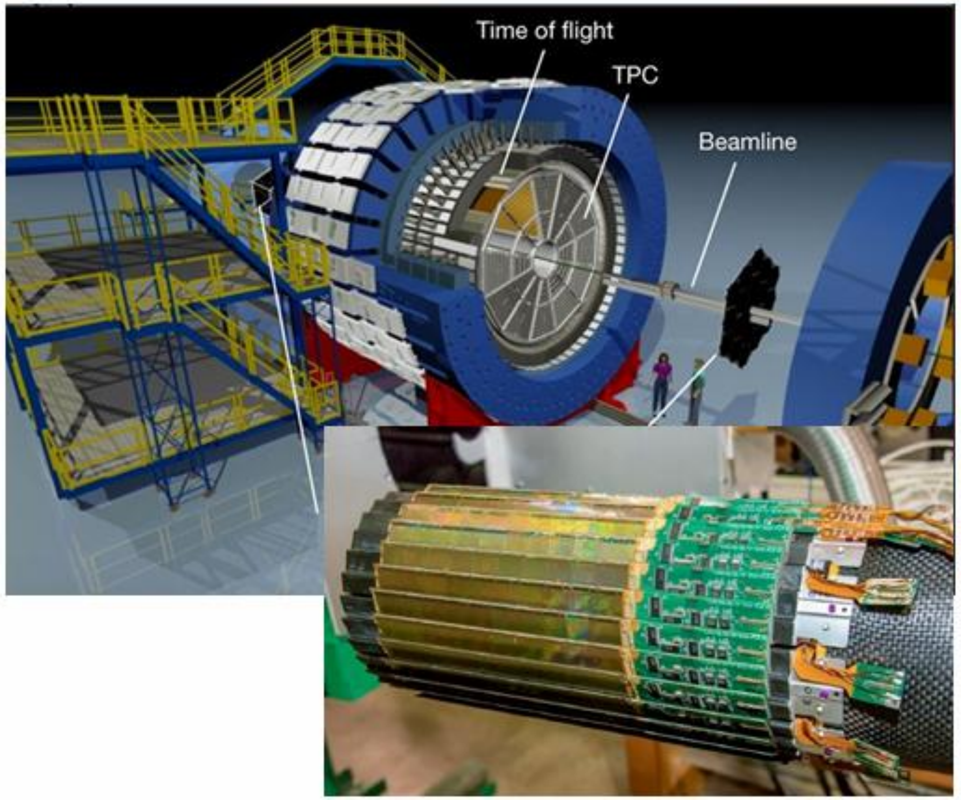
+ smaller readout chip (no bump)

+ issue with back bias, full depletion not (yet) possible (more sensitive to radiation damage)

Epitaxial layer is strinking: ALPIDE 25um, ITS3 10um -> signal reduced accordingly

W. Snoeys, CMOS Monolithic Active Pixel Sensors: challenges and perspectives (6 December 2024) · Indico

FIRST MAPS in HEP: MIMOSA28 (ULTIMATE) in STAR PXL



courtesy of STAR Collaboration

356 M pixels on ~0.16 m² of silicon

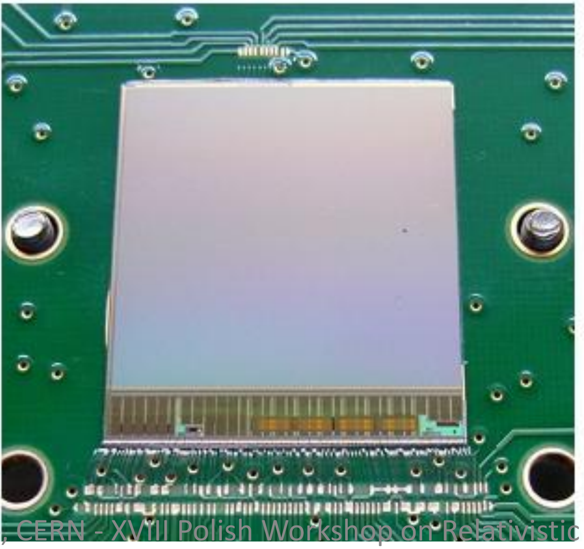
Full detector Jan 2014

Physics Runs in 2015-2016

- 2 layers (2.8 and 8 cm radii)
- 10 sectors total (in 2 halves)
- 4 ladders/sector
- Radiation length (1st layer)
- x/X0 = 0.39% (Al conductor flex)

Ladder with 10 MAPS sensors

2-layer kapton flex cable with Al traces



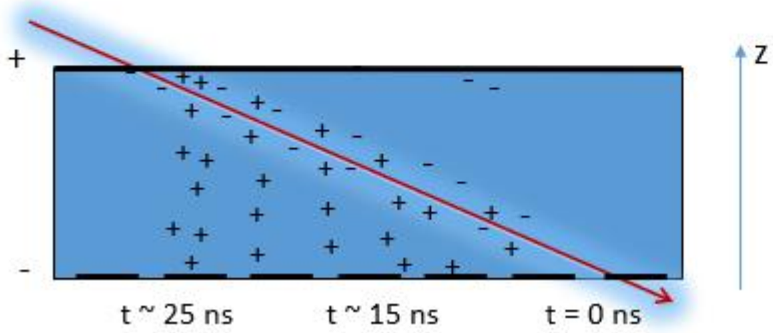
MIMOSA28 (ULTIMATE) – 2011

First MAPS system in HEP

Twin well 0.35 µm CMOS (AMS)

- 18.4 µm pitch
- 576x1152 pixels, 20.2 x 22.7 mm²
- Integration time 190 µs
- No reverse bias -> NIEL ~ 10^{12} n_{eq}/cm^2
- Rolling shutter readout

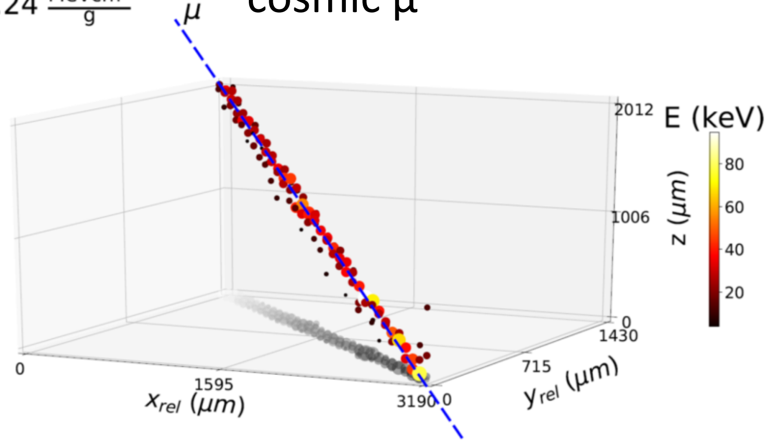
Solid-state Time-Projection Chamber: 3D reconstruction of particle tracks



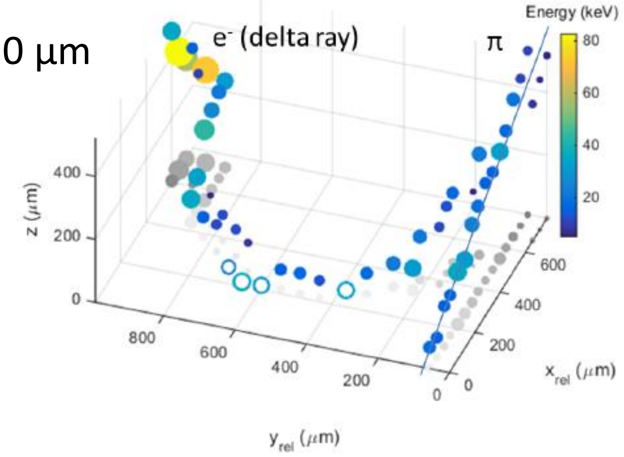
3D track reconstruction – 2 mm CdTe

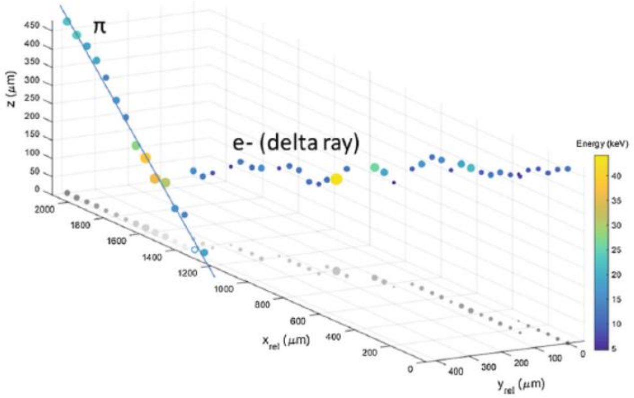
$\frac{dE}{dx} = 1.24\ \frac{\mathrm{MeVcm^2}}{\mathrm{g}}$

cosmic μ



z-resolution: σ_z ~ 30 μm

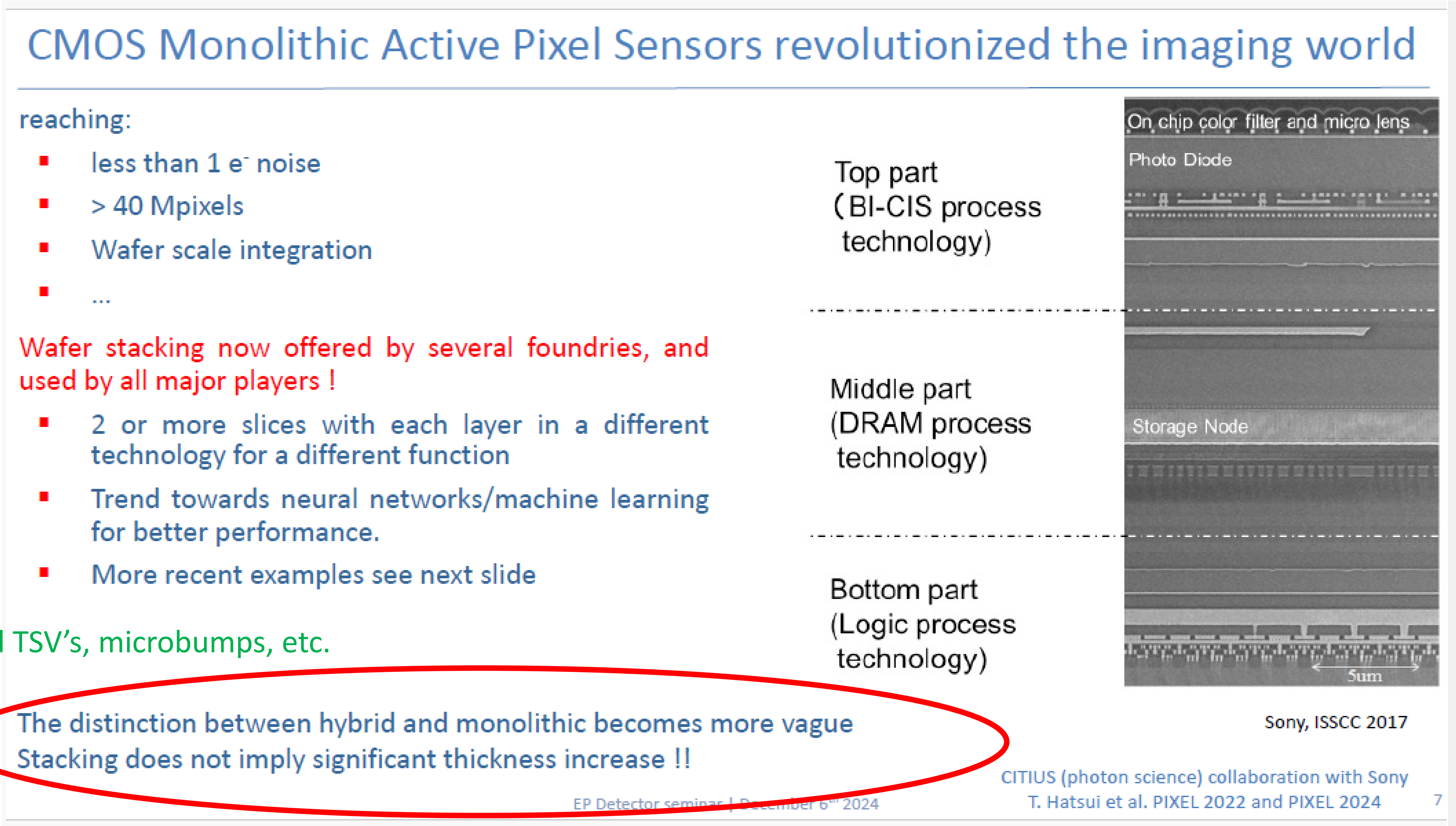




[Particle tracking and identification with single-layer Timepix-series detectors (8 November 2024) · Indico]()

Bergmann et al., Eur. Phys. J. C (2019) 79: 165.
https://doi.org/10.1140/epjc/s10052-019-6673-z

Bergmann et al. Eur. Phys. J. C (2017) 77: 421.
https://doi.org/10.1140/epjc/s10052-017-4993-4



CMOS Monolithic Active Pixel Sensors revolutionized the imaging world

reaching:

- less than 1 e^- noise
- > 40 Mpixels
- Wafer scale integration
- …

Wafer stacking now offered by several foundries, and used by all major players !

- 2 or more slices with each layer in a different technology for a different function
- Trend towards neural networks/machine learning for better performance.
- More recent examples see next slide

And TSV's, microbumps, etc.

The distinction between hybrid and monolithic becomes more vague
Stacking does not imply significant thickness increase !!

Top part
(BI-CIS process
technology)

Middle part
(DRAM process
technology)

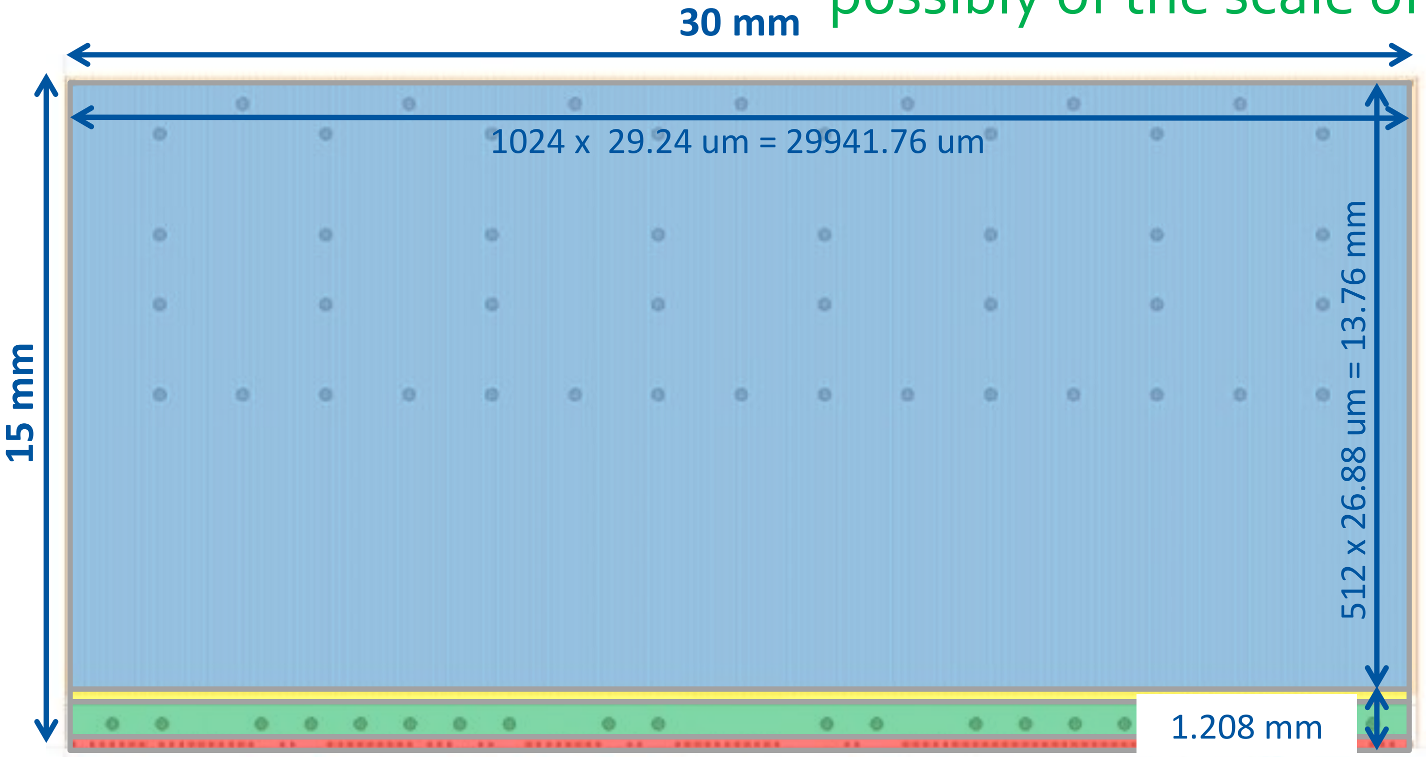
Bottom part
(Logic process
technology)

Sony, ISSCC 2017

CITIUS (photon science) collaboration with Sony
T. Hatsui et al. PIXEL 2022 and PIXEL 2024

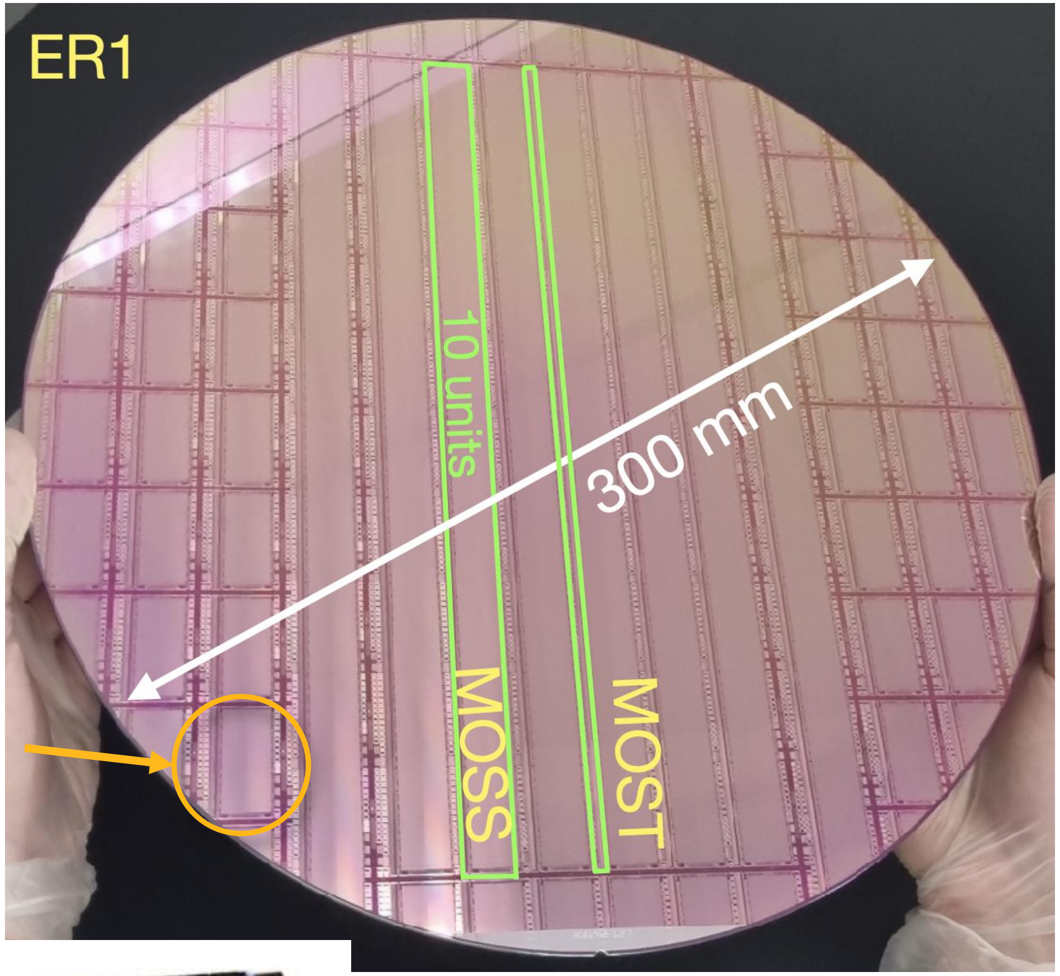
EP Detector seminar | December 6th 2024 7

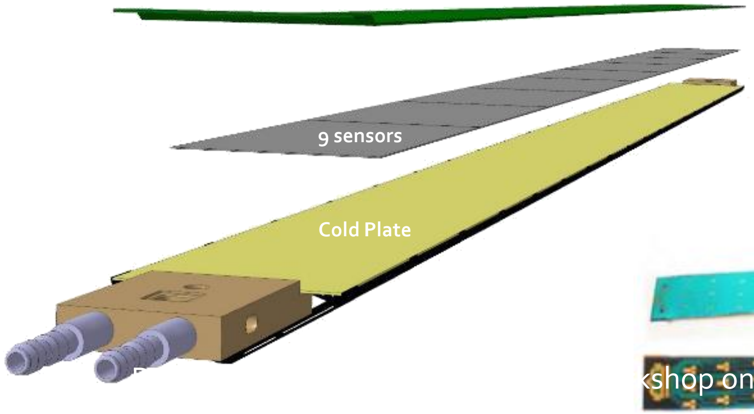
While pixel are getting smaller and smaller, detector are getting larger and larger, possibly of the scale of the Si wafer

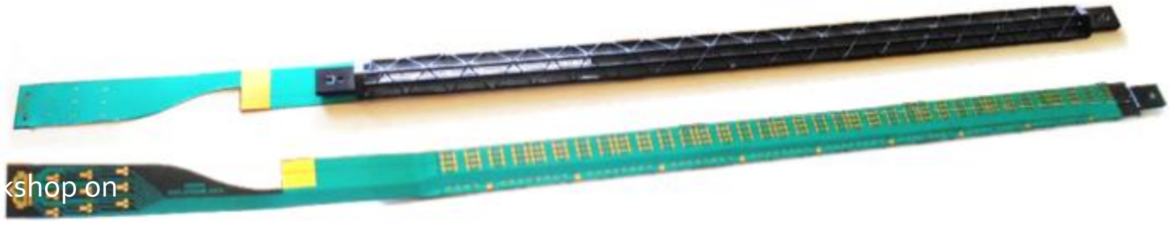


Active area: 92%

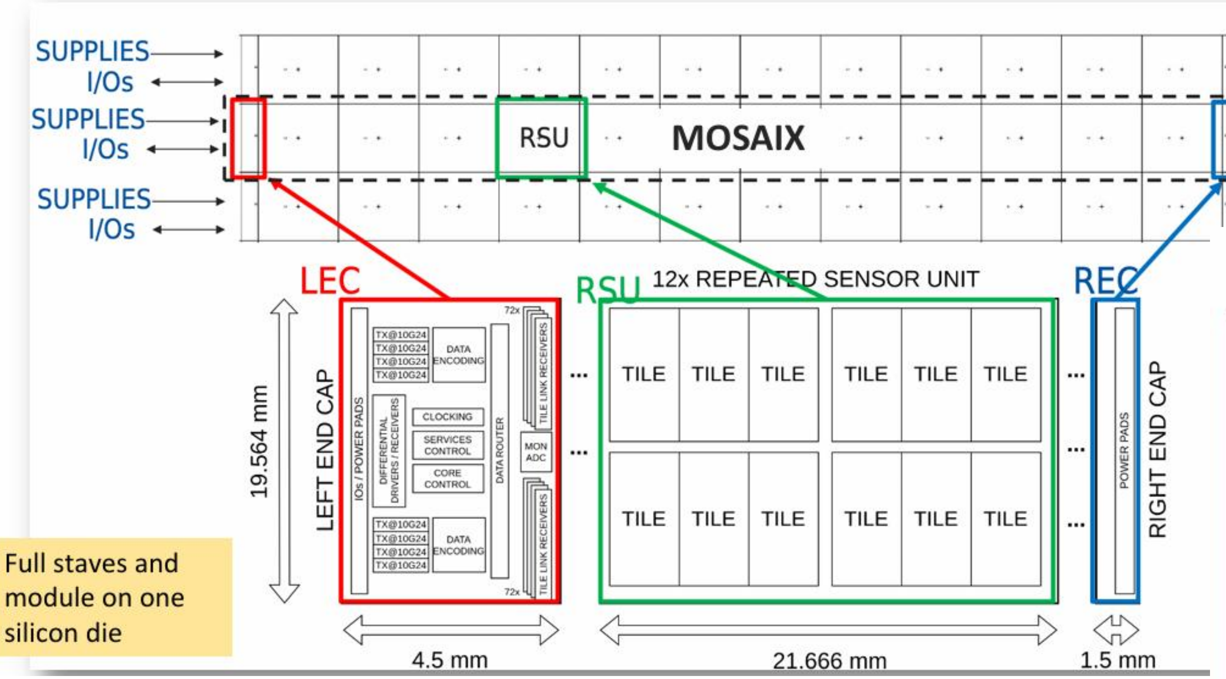
~ ALPIDE



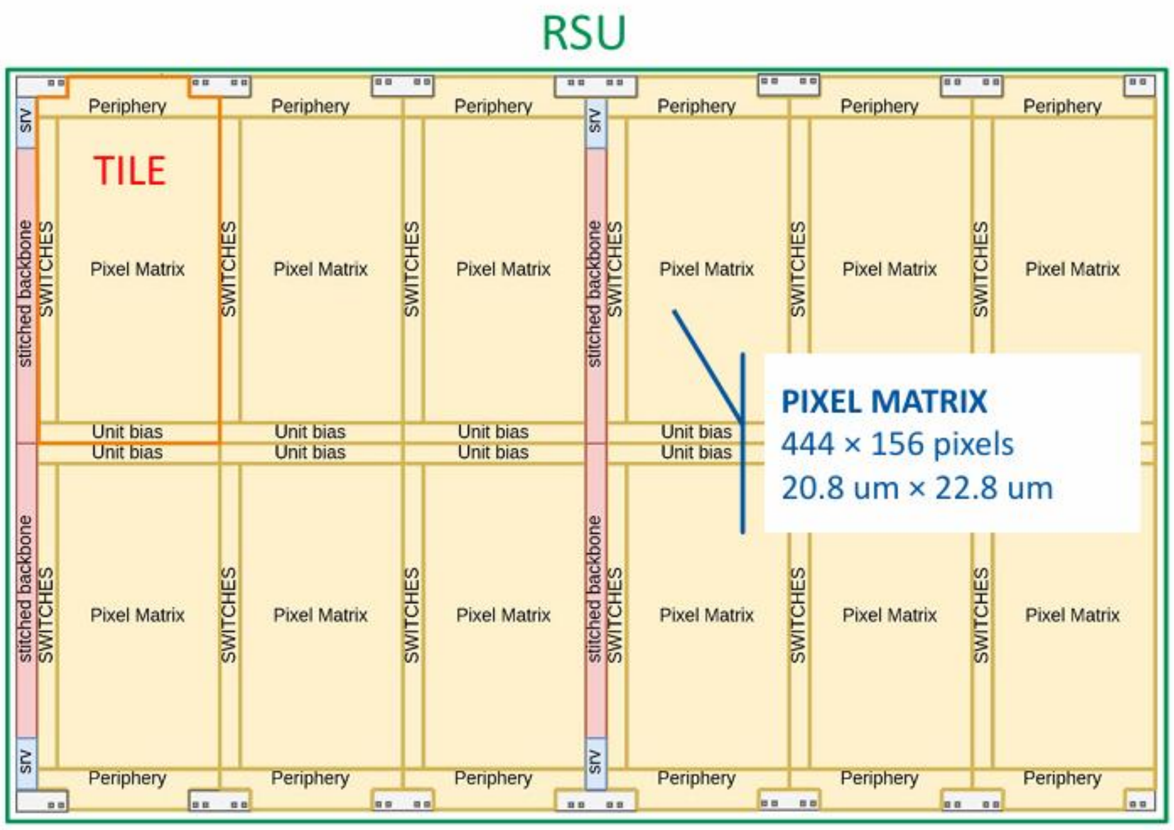




MOSAIX Architecture (ALICE ITS3)



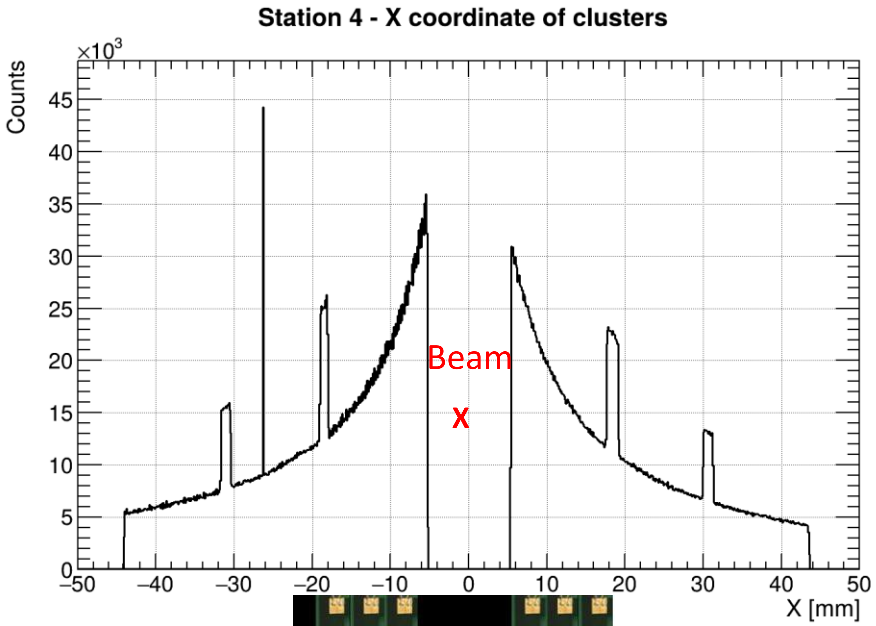
Full staves and module on one silicon die

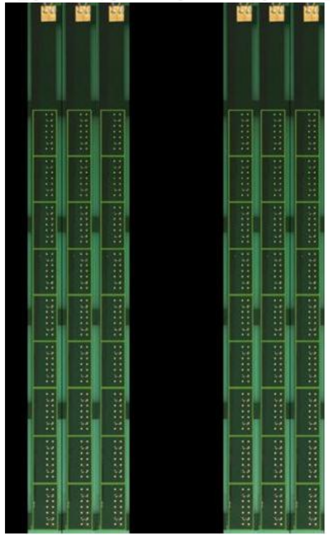


Reduction in sensitive area acceptable for ITS3, may become an issue and require compromize (detector size vs. acceptance)

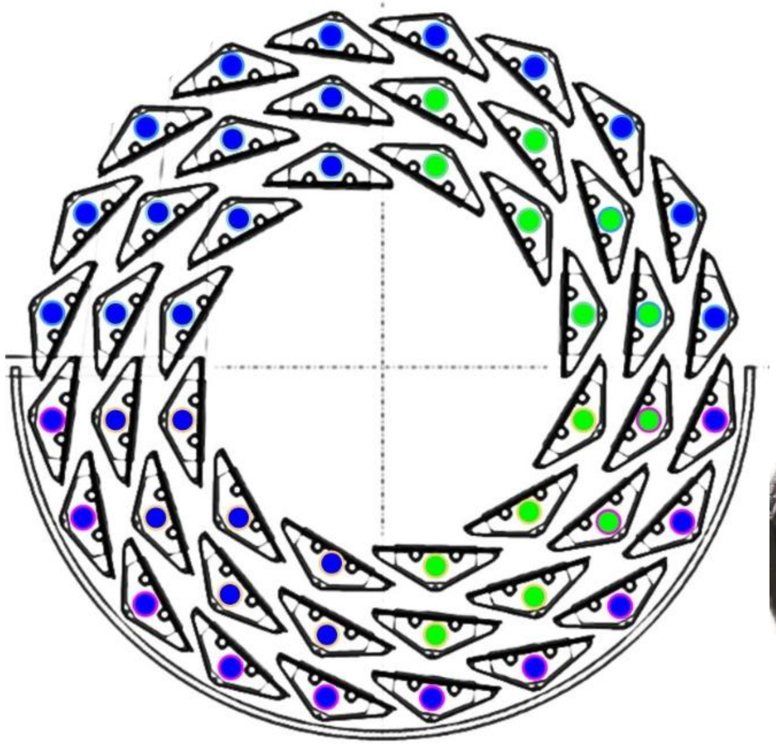
NA61 VD

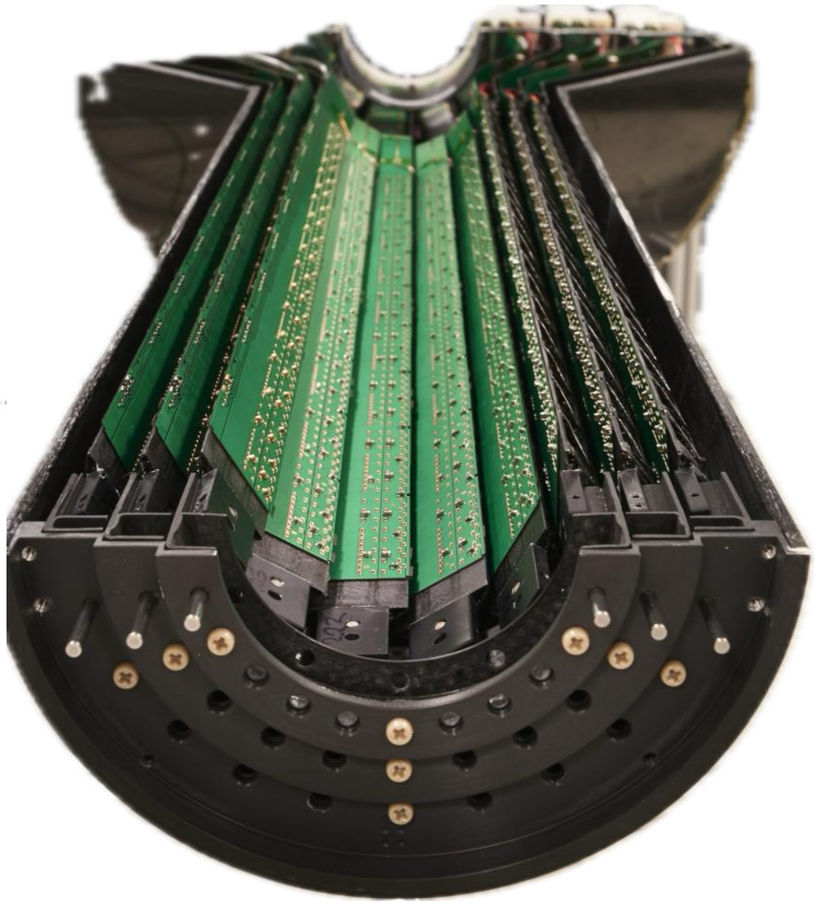
Courtesy Mateusz Bajda





ALICE ITS2 Inner Barrel



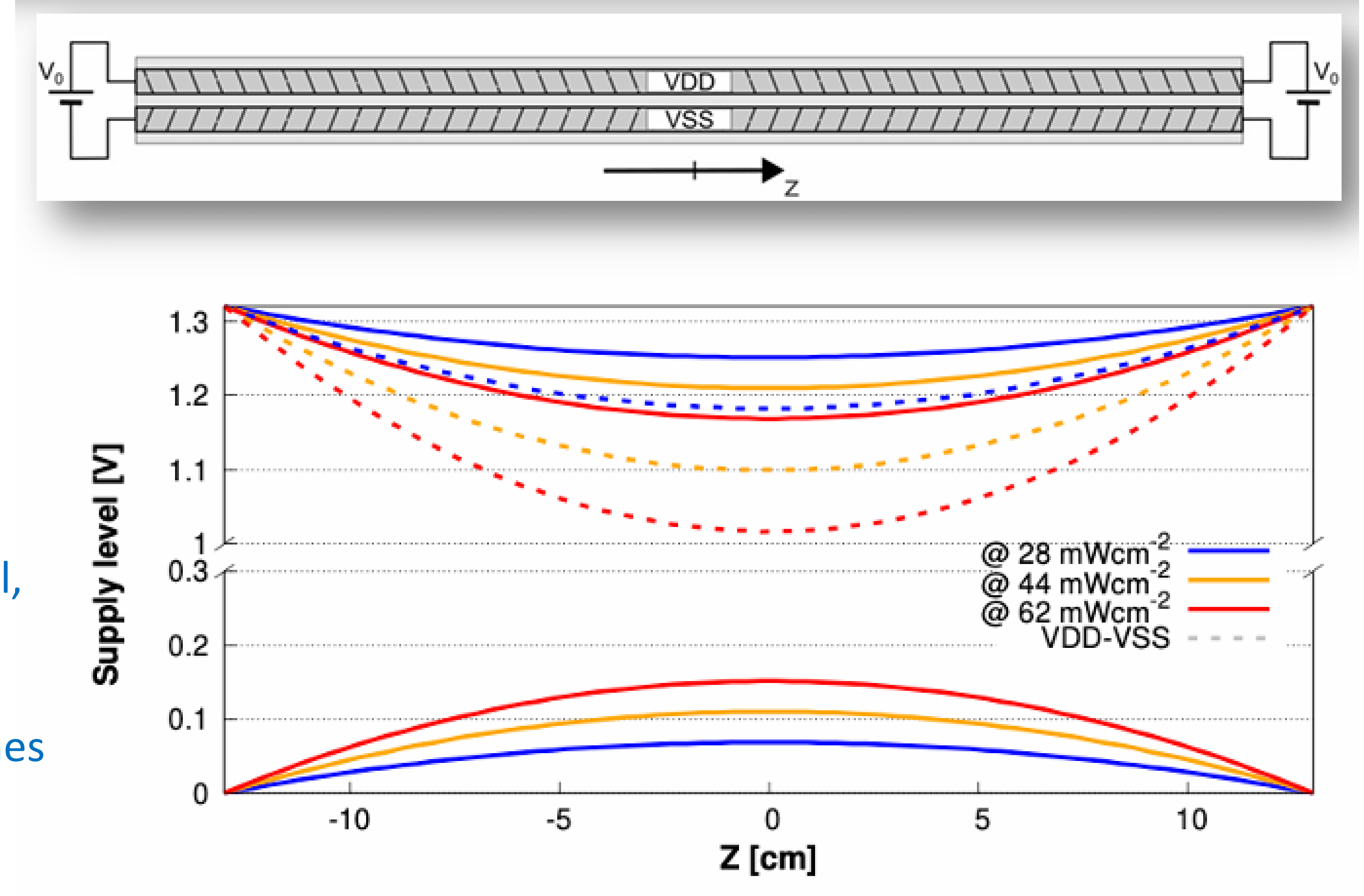


Modularity/overlap allows for recovering 100% acceptance, i.e. hermeticity
Doesn’t work w/ wafer-scale detector: logic/auxiliary services need to be implemented in the detection matrix -> lost of acceptance

In spite of the amazing technological progresses, Ohm's law still hold: V = I x R (and it is expected to hold in the future)

Need additional/thicker metal layer(s)
Still fine for MOSAIX (ALICE ITS3)
but may become a crucial issue for
further developments
(conductivity of metal layers not optimal,
material budget)

External and more conventional power lines
(wires, flex) may be needed



[MAPS detectors technologies for the FCC-ee vertex detector (1-2 July 2024): Overview · Indico](#)
[G. Aglieri Rinella, 20240630-OVERVIEW-MOSAIX-ITS3.pdf](#)

FINAL REMARKS

Silicon Pixel Detectors are at the heart of all HEP, it is even difficult to immagine that 30 years ago they weren't there. And they will play an even more important role in future
(they are even used in calorimetry, for instance ALICE FoCal)

Full exploitation of the latest technologies requires developments at system level (powering, data transmission, mechanical stability to name few) which are very challenging but may not be as appealing as designing the ultimate pixel

Collider environment poses rather different (and more demanding) constraints than Fixed Target,
we should not forget and exploit this

Technological progress is driven by commercial applications, we have to closely monitor the market and find Innovative applications

Basics of microelectronics industry: low-cost mass production

NXP assembly lines
Guandong

they only use own equipment
if > 5-10 x10^9 pieces/year

cost reduction e.g.
by flip-chip bonding

operators??

Erik H.M. HEIJNE
CERN ESE Seminar, 13 March 2028
[Report on IEEE-ISSCC 2018: micro-nano-pico, we must go on (13 March 2018) · Indico]

Thank you for your attention